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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/718,383	11/19/2003	Thomas Joel Massingill		9726

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EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/718,383	MASSINGILL, THOMAS JOEL	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-18* is/are pending in the application.

4a) Of the above claim(s) *2 and 3* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 4 to 18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2/6/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/718383
Filing Date: 11/19/2003;

Applicant: Massingill

Examiner: Alexander Williams

This application claims the benefit of a provisional patent application # 60/460347, filed 4/4/2003.

Applicant's Pre-Amendment filed 2/6/04 has been acknowledged.

Applicant's election of species of figure 3 (claims 1 and 4 to 18), filed 9/26/05, has been acknowledged.

This application contains claims 2 and 3 drawn to an invention non-elected without traverse.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the

invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negatived by the manner in which the invention was made.

Initially, and with respect to claims 1, note that a "product by process" claim is directed to the product per se, no matter how actually made, In re Hirao, 190 USPQ 15 at 17 (footnote 3). See also In re Brown, 173 USPQ 685; In re Luck, 177 USPQ 523; In re Wertheim, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); In re Fitzgerald, 205 USPQ 594, 596 (CCPA); In re Marosi et al., 218 USPQ 289 (CAFC); and most recently, In re Thorpe et al., 227 USPQ 964 (CAFC, 1985) all of which make it clear that it is the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that Applicant has burden of proof in such cases as the above case law makes clear.

Claims 1, 4 to 9, 11, 13 to 15, 17 and 18 are rejected under 35 U.S.C. § 103(a) as being unpatentable over in view of Suzuki et al. (Japan Patent # 11-145322).

1. Suzuki et al. (figures 1 to 3) specifically figure 1 show a semiconductor package **100** comprising an integrated circuit die **101** with a plurality die bond pads **(inherent on the active surface of 101)**, a printed wiring board **102**, with a plurality of package bond pads **107**, with a plurality of package pads, with a plurality of conductive traces 103, or conductive planes, connecting selective package bond pads to respective selected package pads, a recess in the printed wiring board, to attach the die, to contain the plurality of die bond pads and plurality of package bond pads, with the recess containing electrical circuitry, with the recess formed by bending or deforming the printed wiring board, a plurality of electrical connections

between the plurality of die bond pads and the plurality of package bond pads.

4. The package of claim 1, Suzuki et al. show wherein the plurality of electrical connections between the die bond pads and the package bond pads are made by solder balls **BGA (see column 1, paragraph [0002]).**

5. The package of claim 1, Suzuki et al. show wherein the printed wiring board has a metal core, one or more build-up layers and a solder mask passivation layer, where each buildup layer comprises an organic dielectric layer with vias and a patterned metal layer.

6. The package of claim 5, Suzuki et al. show wherein the circuitry of the printed wiring board is on one side, and the printed wiring board does not contain through vias or plated through holes (PTHs).

7. The package of claim 5, Suzuki et al. show wherein the metal core is made from a material which has a TCE to match an electronic board on which the semiconductor package is mounted.

8. The package of claim 7, Suzuki et al. Suzuki et al. show wherein the material is copper or aluminum.

9. The package of claim 5, Suzuki et al. show wherein the metal core is made from a material with a TCE to match the integrated circuit die.

11. The package of claim 5, Suzuki et al. show wherein the metal core is made from a material with a TCE half way between the integrated circuit die and the electronic board on which the semiconductor package is mounted.

13. The package of claim 1, Suzuki et al. show wherein the plurality of package pads are arranged in an array, where the array need not be fully populated with package pads and particularly the center of the array is not populated with package pads.

14. The package of claim 13, Suzuki et al. show wherein the pitch of the array, the distance from the center of one package pad to the center of an adjacent populated package pad is 0.5 mm, 0.65 mm, 0.8 mm, 1.0 mm and 1.27 mm.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

15. The package of claim 13, Suzuki et al. show wherein there are a plurality of package solder balls **104** attached to respective selected package pads.

17. The package of claim 1, Suzuki et al. show wherein the plurality of package pads are arranged in one, two or more rows around the perimeter of the printed wiring board.

18. The package of claim 17, Suzuki et al. show wherein the pitch of the package pads, the distance from the center of one package pad to the center of an adjacent package pad is 0.5 mm, 0.65 mm, 0.8 mm, 1.0 mm and 1.27 mm.

Note that the specification contains no disclosure of either the critical nature of the claimed dimensions or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the Applicant must show that the chosen dimensions are critical. In re Woodruff, 919 F.2d 1575, 1578, 16 USPQ2d 1934, 1936 (Fed. Cir. 1990).

As to the grounds of rejection under section 103, see MPEP § 2113.

Claim 16 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Suzuki et al. (Japan Patent # 11-145322) in view of Minami et al. (Japan Patent # 4-133342).

Suzuki et al. show the features of the claimed invention as detailed above, but fail to explicitly show there are a plurality of package pins attached to respective selected package pads.

Minami et al. show a semiconductor package. Specifically, Minamo et al. (figures 1 to 4)

specifically figure 2 discloses a recessed part substrate **14** and a semiconductor chip **7**, wherein there are a plurality of package pins **4** attached to respective selected package pads for the purpose of attaching a terminal pin to a package substrate.

16. The package of claim 13, the combination with Minami et al. show wherein there are a plurality of package pins attached to respective selected package pads.

Therefore, it would have been obvious to one of ordinary skill in the art to use Minami et al.'s pin terminals to modify Suzuki et al.'s ball terminals for the purpose attaching a terminal pin to a package substrate.

Claim 10 and 12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Suzuki et al. (Japan Patent # 11-145322) in view of Nishihara et al. (U.S. Patent # 5,639,990).

Suzuki et al. show the features of the claimed invention as detailed above, but fail to explicitly show the material is CuW, Mo, CuMo, copper clad Mo, Invar, and copper clad Invar and wherein the material is stainless steel.

Nishihara et al. show a solid printed substrate and electronic circuit package. Specifically, Nishihara et al. (figures 1 to 10C) specifically figure 10C discloses the board being of the material is CuW, Mo, CuMo, copper clad Mo, Invar, and copper clad Invar and wherein the material is stainless steel for the purpose of attaching a terminal pin to a package substrate.

10. The package of claim 9, the combination with Nishihara et al. show wherein the material is CuW, Mo,

CuMo, copper clad Mo, Invar, and copper clad Invar and wherein the material is stainless steel.

12. The package of claim 11, the combination of Nishihara et al. show wherein the material is stainless steel.

(22) Although the metal board of the solid printed substrate of the present invention is generally 0.05 to 2.0 mm in thickness, preferably a board made of aluminum, copper alloy such as nickel silver or brass, copper, copper clad invar, stainless steel, iron, silicon steel and aluminum processed by electrolytic oxidation or the like, each being 0.1 to 1.5 mm thick, can be used. With the metal board thinner than 0.05 mm thick, the flatness of the surface is degraded after final machining and hence workability of wire bonding in packaging of electronic parts is lowered. Further, with the metal board thicker than 2.0 mm, though simple bending work can be executed without any obstacle, It becomes difficult to process the board by deep drawing.

Therefore, it would have been obvious to one of ordinary skill in the art to use Nishihara et al.'s board material to modify Suzuki et al.'s substrate material for the purpose attaching a terminal pin to a package substrate.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/668,734,737,738,691,690,602,693,697,698,666,783,707,712,713,717,720,706,703,702,699,786,784,676,675	10/15/05
Other Documentation: foreign patents and literature in 257/668,734,737,738,691,690,602,693,697,698,666,783,707,712,713,717,720,706,703,702,699,676,675	10/15/05
Electronic data base(s): U.S. Patents EAST	10/15/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
10/15/05